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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/583,427	05/10/2007	Cedric Thebault	PD030135	1698
24498 7590 12/11/2009 Robert D. Shedd, Patent Operations THOMSON Licensing LLC P.O. Box 5312 Princeton, NJ 08543-5312				
EXAMINER XAVIER, ANTONIO J				
ART UNIT		PAPER NUMBER		
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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary

Application No.

10/583,427

Applicant(s)

THEBAULT ET AL.

Examiner

ANTONIO XAVIER

Art Unit

2629

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --
Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) ☒ Responsive to communication(s) filed on 19 June 2006.
- 2a) ☐ This action is **FINAL**. 2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) ☒ Claim(s) 1-7 is/are pending in the application.
- 4a) Of the above claim(s) _____ is/are withdrawn from consideration.
- 5) ☐ Claim(s) _____ is/are allowed.
- 6) ☒ Claim(s) 1-7 is/are rejected.
- 7) ☐ Claim(s) _____ is/are objected to.
- 8) ☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

- 9) ☒ The specification is objected to by the Examiner.
- 10) ☒ The drawing(s) filed on 19 June 2006 is/are: a) ☒ accepted or b) ☐ objected to by the Examiner.
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

- 12) ☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☒ All b) ☐ Some * c) ☐ None of:
1. ☒ Certified copies of the priority documents have been received.
 2. ☐ Certified copies of the priority documents have been received in Application No. _____.
 3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

- 1) ☒ Notice of References Cited (PTO-892)
- 2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
- 3) ☒ Information Disclosure Statement(s) (PTO/SB/226)
- 4) ☐ Interview Summary (PTO-413)
- 5) ☐ Notice of Informal Patent Application
- 6) ☐ Other: _____
- Paper No(s)/Mail Date 6/19/06

DETAILED ACTION

Specification

Claim Rejections - 35 USC § 112

1. The following is a quotation of the second paragraph of 35 U.S.C. 112:

The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

2. Claims 1-7 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

Examiner notes that Applicant appears to be using a definition for the term "extrapolation" that is significantly different from the generally accepted meaning.

Where applicant acts as his or her own lexicographer to specifically define a term of a claim contrary to its ordinary meaning, the written description must clearly redefine the claim term and set forth the uncommon definition so as to put one reasonably skilled in the art on notice that the applicant intended to so redefine that claim term. *Process Control Corp. v. HydReclaim Corp.*, 190 F.3d 1350, 1357, 52 USPQ2d 1029, 1033 (Fed. Cir. 1999). The term "extrapolation" in Claim 1 is used by the claim to mean

"approximating values between two known values (more commonly known as interpolation)," while the accepted meaning is "approximating values beyond known values." The term is indefinite because the specification does not clearly redefine the term.

Examiner notes paragraph [0043] of U.S. Pub. No.: 2007/0222707 (or page 7, lines 10-21 of the specification as filed on June 19, 2006) teaches bound points are used. The primary APL value is the highest APL value and the secondary APL value is the lowest APL value. Furthermore, the LUT generation described in paragraph [0079] (or page 10, line 20-page 11, line 4) teaches the metacode LUTs between the primary and secondary APL values are computed (emphasis added).

Claims 2-7 depend on Claim 1 and are rejected for substantially the same reasons.

3. Claims 4-5 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

Examiner notes that Claim 4 is a method that is dependent on a device.

Examiner notes that Claim 5 is a device that is dependent on a method that is dependent on a device.

Claim 4 has not been examined on the merits.

Claim Rejections - 35 USC § 102

4. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

5. Claims 1-3 and 5-7 are rejected under 35 U.S.C. 102(b) as being anticipated by Lee (U.S. Pub. No.: 2003/0098839).

With respect to Claim 1, Lee teaches a device for generating a look-up table for a given value of a parameter among N different values, whose output values can be approximated by a piecewise linear function of a variable depending on the given value, the set of N values being divided into P subsets of consecutive values, each piece of the piecewise linear function being in a different subset, wherein it comprises (Examiner is **not giving patentable weight** to the intended use recited in the preamble because it does not limit the device to a particular structure):

a first memory (Fig. 9, item 441) for storing, for each subset i, a primary look-up table associated to a bound value of the subset i (Examiner is **not giving patentable weight** to the intended use because it does not limit the device to a particular structure),

a second memory (Fig. 9, item 441) for storing, for each subset i , a delta look-up table corresponding to the difference between a secondary look-up table and the primary look-up table related to the subset i , the secondary look-up table being associated to the other bound value of the subset i (Examiner is **not giving patentable weight** to the intended use because it does not limit the device to a particular structure),

a third memory (Fig. 9, item 441) for storing, for each of said N values, an index indicating which primary look-up table in the first memory and which delta look-up table in the second memory have to be used for extrapolation (Examiner is **not giving patentable weight** to the intended use because it does not limit the device to a particular structure),

a fourth memory (Fig. 9, item 441) for storing an extrapolation coefficient for each one of said N values, the extrapolation coefficient associated to a given value being defined in accordance with the value of a variable S for said given value and the values of the variable S for the two bound values of the subset i comprising said given value (Examiner is **not giving patentable weight** to the intended use because it does not limit the device to a particular structure); and

a computing block (Fig. 9, item 443) for generating a look-up table, for the given value in accordance with the related extrapolation coefficient, primary look-up table and delta look-up table (Examiner is **not giving patentable weight** to the intended use because it does not limit the device to a particular structure).

Examiner notes that the broadest reasonable interpretation of the first through fourth memory does not require four separate memory devices. A single memory device (for example RAM) can contain four memory locations or be partitioned. Examiner further notes that the claims as written are extremely broad and read on any computer (CPU + memory). If Applicant intends to claim four separate memory devices then Examiner highly recommends describing specific structure to distinguish the memory, how the memory is connected, how the signal lines transfer data or something along those lines so as to distinguish the structure as it relates to this device.

Examiner further notes that the broadest reasonable interpretation of the computing block does not require a specific CPU or logic device. Any CPU or logic device is capable of generating a look-up table. Examiner further notes that the claims as written are extremely broad and read on any computer (CPU + memory). If Applicant intends to claim a specific computing block device then Examiner highly recommends describing specific structure.

With respect to Claim 2, Lee teaches a device according to Claim 1, discussed above, wherein the parameter is an average power level and the variable is a number of sustain pulses corresponding to the given value of the parameter (Examiner is **not giving patentable weight** to the intended use because it does not limit the device to a particular structure)

and a Metacode look-up table for each average power level value (Examiner is **not giving patentable weight** to the intended use because it does not limit the device to a particular structure).

Examiner notes the broadest reasonable interpretation of a device with specific data does not require specific changes to the memory structure. Examiner notes that a device claiming the specific data located in the memory structure is generally considered arbitrary and does not require any specific structure. Memory is capable of storing data and data can be any arbitrary item including, but not limited to, an average power level or the number of sustain pulses. Although it may be possible to claim the data with enough specificity to require specific structure (i.e., specific number of bits) the claim as currently written is extremely broad and reads on all memory.

The further limitations of Claims 3 and 5-7 are rejected for substantially the same reasons as Claim 2, discussed above.

6. Claims 1-3 and 5-7 are rejected under 35 U.S.C. 102(b) as being anticipated by Akiyama (U.S. Pat. No.: 4,901,258).

With respect to Claim 1, Akiyama teaches a device for generating a look-up table for a given value of a parameter among N different values, whose output values can be

approximated by a piecewise linear function of a variable depending on the given value, the set of N values being divided into P subsets of consecutive values, each piece of the piecewise linear function being in a different subset, wherein it comprises (Examiner is **not giving patentable weight** to the intended use recited in the preamble because it does not limit the device to a particular structure):

a first memory (Fig. 1, item 9) for storing, for each subset i, a primary look-up table associated to a bound value of the subset i (Examiner is **not giving patentable weight** to the intended use because it does not limit the device to a particular structure),

a second memory (Fig. 1, item 9) for storing, for each subset i, a delta look-up table corresponding to the difference between a secondary look-up table and the primary look-up table related to the subset i, the secondary look-up table being associated to the other bound value of the subset i (Examiner is **not giving patentable weight** to the intended use because it does not limit the device to a particular structure),

a third memory (Fig. 1, item 9) for storing, for each of said N values, an index indicating which primary look-up table in the first memory and which delta look-up table in the second memory have to be used for extrapolation (Examiner is **not giving patentable weight** to the intended use because it does not limit the device to a particular structure),

a fourth memory (Fig. 1, item 11) for storing an extrapolation coefficient for each one of said N values, the extrapolation coefficient associated to a given value being defined in accordance with the value of a variable S for said given value and the values of the variable S for the two bound values of the subset i comprising said given value

(Examiner is **not giving patentable weight** to the intended use because it does not limit the device to a particular structure); and

a computing block (Fig. 1, item 8) for generating a look-up table, for the given value in accordance with the related extrapolation coefficient, primary look-up table and delta look-up table (Examiner is **not giving patentable weight** to the intended use because it does not limit the device to a particular structure).

As discussed above, Examiner notes that the broadest reasonable interpretation of the first through fourth memory does not require four separate memory devices.

As discussed above, Examiner further notes that the broadest reasonable interpretation of the computing block does not require a specific CPU or logic device.

With respect to the inventive concept of saving memory by using a reduced LUT and interpolating the missing data to generate a larger LUT, Examiner directs Applicant to Abstract, Col. 1, lines 50-65 and Col. 3, line 15-Col. 4, line 23.

With respect to Claim 2, Akiyama teaches a device according to Claim 1, discussed above, wherein the parameter is an average power level and the variable is a number of sustain pulses corresponding to the given value of the parameter (Examiner is **not giving patentable weight** to the intended use because it does not limit the device to a particular structure)

and a Metacode look-up table for each average power level value (Examiner is **not giving patentable weight** to the intended use because it does not limit the device to a particular structure).

As discussed above, Examiner notes the broadest reasonable interpretation of a device with specific data does not require specific changes to the memory structure.

The further limitations of Claims 3 and 5-7 are rejected for substantially the same reasons as Claim 2, discussed above.

7. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

8. Claims 1-3 and 5-7 are rejected under 35 U.S.C. 102(e) as being anticipated by Kuhns (U.S. Pat. No.: 7,382,349)

With respect to Claim 1, Kuhns teaches a device for generating a look-up table for a given value of a parameter among N different values, whose output values can be approximated by a piecewise linear function of a variable depending on the given value, the set of N values being divided into P subsets of consecutive values, each piece of the piecewise linear function being in a different subset, wherein it comprises (Examiner is **not giving patentable weight** to the intended use recited in the preamble because it does not limit the device to a particular structure):

a first memory (Fig. 1, item 118) for storing, for each subset i , a primary look-up table associated to a bound value of the subset i (Examiner is **not giving patentable weight** to the intended use because it does not limit the device to a particular structure),

a second memory (Fig. 1, item 118) for storing, for each subset i , a delta look-up table corresponding to the difference between a secondary look-up table and the primary look-up table related to the subset i , the secondary look-up table being associated to the other bound value of the subset i (Examiner is **not giving patentable weight** to the intended use because it does not limit the device to a particular structure),

a third memory (Fig. 1, item 118) for storing, for each of said N values, an index indicating which primary look-up table in the first memory and which delta look-up table in the second memory have to be used for extrapolation (Examiner is **not giving patentable weight** to the intended use because it does not limit the device to a particular structure),

a fourth memory (Fig. 1, item 118) for storing an extrapolation coefficient for each one of said N values, the extrapolation coefficient associated to a given value being

defined in accordance with the value of a variable S for said given value and the values of the variable S for the two bound values of the subset i comprising said given value (Examiner is **not giving patentable weight** to the intended use because it does not limit the device to a particular structure); and

a computing block (Fig. 1, item 116) for generating a look-up table, for the given value in accordance with the related extrapolation coefficient, primary look-up table and delta look-up table (Examiner is **not giving patentable weight** to the intended use because it does not limit the device to a particular structure).

As discussed above, Examiner notes that the broadest reasonable interpretation of the first through fourth memory does not require four separate memory devices.

As discussed above, Examiner further notes that the broadest reasonable interpretation of the computing block does not require a specific CPU or logic device.

With respect to the inventive concept of saving memory by using a reduced LUT and interpolating the missing data to generate a larger LUT, Examiner directs Applicant to Col. 3, line 65-Col. 4, line 2 and Col. 4, line 61-Col. 5, line 26.

With respect to Claim 2, Kuhns teaches a device according to Claim 1, discussed above, wherein the parameter is an average power level and the variable is a number of sustain pulses corresponding to the given value of the parameter (Examiner is **not**

giving patentable weight to the intended use because it does not limit the device to a particular structure)

and a Metacode look-up table for each average power level value (Examiner is **not giving patentable weight** to the intended use because it does not limit the device to a particular structure).

As discussed above, Examiner notes the broadest reasonable interpretation of a device with specific data does not require specific changes to the memory structure.

The further limitations of Claims 3 and 5-7 are rejected for substantially the same reasons as Claim 2, discussed above.

Conclusion

9. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. Correa et al. (U.S. Pub. No.: 2003/0201952) teaches metacodes, multiple LUTs and interpolation with sustain pulses. Duvanenko et al. (U.S. Pat. No.: 5,951,625) teaches interpolated LUTs.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to ANTONIO XAVIER whose telephone number is 571-270-7688. The examiner can normally be reached on M-Th 9:30am-4:30pm EST.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Amare Mengistu can be reached on 571-272-7674. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/A. X./
Examiner, Art Unit 2629

/Amare Mengistu/
Supervisory Patent Examiner, Art Unit 2629